AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

LISTING OF CLAIMS:

1 – 48. (Cancelled without prejudice or disclaimer)

49. (New) A semiconductor device comprising:

a semiconductor substrate;

an element isolating region having a trench formed in said semiconductor substrate and an insulating film which is embedded into said trench; and

an active region formed in said semiconductor substrate and including a well region in which a gate insulating film is formed thereon and a gate electrode is formed on the gate insulating film, said well region having ion implanted source and drain diffusion regions provided in correspondence to said gate electrode,

wherein the embedded insulating film in said trench has a bottom surface plane extended deeper into said semiconductor substrate than said diffusion regions and surrounds said active region, in a plan view thereof,

wherein the embedded insulating film has a recessed upper plane surface surrounding at least said source and drain diffusion regions to prevent crystalline defects caused by said element isolation region at vicinity of said diffusion regions, the recessed upper plane surface defining a depth, extended from a plane surface of said semiconductor substrate, substantially the same as or greater than that of the depth of the peak concentration of the impurity profile of each of said source and drain diffusion regions, and

wherein an oxynitride film is formed along side and bottom surface planes of

the embedded insulating film in said trench and interfacing with said silicon substrate.

50. (New) A semiconductor device as claimed in claim 49 wherein:

a thermal oxide film is provided along both bottom and sidewall of said trench and said oxynitride film is formed along side and bottom surface planes of said thermal oxide film interfacing with said silicon substrate.

51. (New) A semiconductor device as claimed in claim 49 wherein:

said depth of said recessed upper plane surface is larger than a thickness of said gate insulating film.

52. (New) A semiconductor device as claimed in claim 49 wherein:

said depth of said recessed upper plane surface is larger than a distance defined from a surface of said semiconductor substrate to said depth where the impurity profile of said ion implanted source and drain regions is at peak concentration.

53. (New) A semiconductor device as claimed in claim 49 wherein:

said embedding insulating film has a recessed upper plane surface throughout said trench except where said gate electrode is positioned.

54. (New) A semiconductor device as claimed in claim 49 wherein:

the recessed upper plane surface defines a depth measured from a location on said plain surface of the substrate midway between an edge of the gate electrode

and the near sidewall of the trench.

55. (New) A semiconductor device comprising:

a semiconductor substrate including a plurality of active regions where elements are formed in a well region, and an element isolating region for mutually isolating said plural active regions from each other;

a gate electrode formed via a gate insulating film on a surface of each of the active regions of said semiconductor substrate, wherein each element of an active region has ion implanted source and drain diffusion regions provided in correspondence to said gate electrode thereof; and

a trench formed in the element isolating region of said semiconductor substrate, into which an insulating film is embedded,

wherein the embedded insulating film in said trench has a bottom surface plane extended deeper into said semiconductor substrate than said diffusion regions and surrounds each of said active regions, in a plan view thereof,

wherein the embedded insulating film has a recessed upper plane surface surrounding at least said source and drain diffusion regions to prevent crystalline defects caused by said element isolation region at vicinity of said diffusion regions, the recessed upper plane surface defining a depth, extended from a plane surface of said semiconductor substrate, substantially the same as or greater than that of the depth of the peak concentration of the impurity profile of each of said source and drain diffusion regions, and

wherein an oxynitride film is formed along side and bottom surface planes of the embedded insulating film in said trench and interfacing with said silicon substrate.

56. (New) A semiconductor device as claimed in claim 55 wherein:

a thermal oxide film is provided along both bottom and sidewall of said trench and said oxynitride film is formed along side and bottom surface planes of said thermal oxide film interfacing with said silicon substrate.

57. (New) A semiconductor device as claimed in claim 55 wherein:

said depth of said recessed upper plane surface is larger than a thickness of said gate insulating film.

58. (New) A semiconductor device as claimed in claim 55 wherein:

said depth of said recessed upper plane surface is larger than a distance defined from a surface of said semiconductor substrate to said depth where the impurity profile of said ion implanted source and drain regions is at peak concentration.

59. (New) A semiconductor device as claimed in claim 55 wherein:

said embedding insulating film has a recessed upper plane surface throughout said trench except where said gate electrode is positioned.

60. (New) A semiconductor device as claimed in claim 55 wherein:

the recessed upper plane surface defines a depth measured from a location on said plain surface of the substrate midway between an edge of the gate electrode and the near sidewall of the trench.